

1 151. (Amended) A synchronous memory device including an array
2 of memory cells, the synchronous memory device comprises:
3 clock receiver circuitry to receive an external clock signal;
4 input receiver circuitry to sample a first operation code in
5 response to a rising edge transition of the external clock signal;
6 a programmable register to store a value which is
7 representative of an amount of time to transpire before the memory
8 device outputs data, wherein the memory device stores the value in
9 the programmable register in response to the first operation code;
10 and
11 output driver circuitry to output data in response to a second
12 operation code, wherein the data is output after the amount of time
13 transpires, and wherein:
14 the output driver circuitry outputs a first portion of
15 the data synchronously with respect to a rising edge
16 transition of the external clock signal and outputs a second
17 portion of the data synchronously with respect to a falling
18 edge transition of the external clock signal.

1 152. The memory device of claim 151 wherein the first
2 operation code is included in a control register access packet.

1 153. The memory device of claim 152 wherein the first
2 operation code and the value are included in the same control
3 register access packet.

1 154. (Amended) The memory device of claim 151 wherein the
2 memory device is a synchronous dynamic random access memory.

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1 155. (Amended) The memory device of claim 151 wherein the
2 input receiver circuitry receives the second operation code and
3 address information.

1 156. (Amended) The memory device of claim 155 wherein the
2 input receiver circuitry receives the second operation code and the
3 address information on consecutive clock cycles of the external
4 clock signal.

1 157. (Amended) The memory device of claim 151 wherein the
2 amount of time is a number of clock cycles of the external clock
3 signal.

1 158. The memory device of claim 151 wherein the input receiver
2 circuitry receives a third operation code, wherein the third
3 operation code initiates a write operation in the memory device.

1 159. (Amended) The memory device of claim 158 wherein the
2 input receiver circuitry receives the third operation code and
3 address information.

1 160. (Amended) The memory device of claim 151 further
2 including delay lock loop circuitry coupled to the clock receiver
3 circuitry to generate a first internal clock signal, wherein the
4 data is output in response to the first internal clock signal.

1 161. The memory device of claim 151 wherein the output driver
2 circuitry outputs the data onto a bus.

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1 162. (Amended) The memory device of claim 161 wherein the bus
2 includes a set of signal lines to carry multiplexed address
3 information, data and control information.

1 163. (Amended) A method of operation of a synchronous memory
2 device, wherein the memory device includes an array of memory cells
3 and a programmable register, the method of operation of the memory
4 device comprises:

5 sampling a first operation code synchronously with respect to
6 an external clock signal;

7 receiving a binary value which is representative of an amount
8 of time to transpire before the memory device outputs data in
9 response to a second operation code wherein the memory device
10 stores the binary value in the programmable register in response to
11 the first operation code;

12 sampling the second operation code; and

13 outputting the data after the amount of time transpires,
14 wherein a first portion of the data is output synchronously with
15 respect to a first transition of the external clock signal and a
16 second portion of the data is output synchronously with respect to
17 a second transition of the external clock signal.

1 164. The method of claim 163 wherein the second operation code
2 is sampled synchronously with respect to the external clock signal.

1 165. The method of claim 163 wherein the binary value is
2 representative of a number of clock cycles of the external clock
3 signal.

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1 166. The method of claim 165 further including:
2 receiving block size information wherein the block size
3 information defines an amount of data to be output in response to
4 the second operation code, wherein the memory device outputs the
5 amount of data after the number of clock cycles of the external
6 clock signal transpire.

1 167. The method of claim 163 further including ^{Sampling}~~receiving~~
2 address information synchronously with respect to the external
3 clock signal.

1 168. The method of claim 163 wherein the address information
2 and the second operation code are included in a read request
3 packet.

1 169. The method of claim 163 further including receiving
2 precharge information.

1 170. The method of claim 169 wherein the precharge information
2 includes a binary bit, wherein, after accessing the data from the
3 array of memory cells, the memory device retains contents of a
4 plurality of sense amplifiers for a subsequent memory operation as
5 a result of a first state of the binary bit.

1 171. The method of claim 163 wherein the first transition of
2 the external clock signal is a rising edge transition and the
3 second transition of the external clock signal is a falling edge
4 transition.

1 172. The method of claim 171 wherein the first and second
2 transitions of the external clock signal are consecutive
3 transitions of the external clock signal.

1 173. The method of claim 163 wherein the first operation code
2 is sampled during an initialization sequence after power is applied
3 to the memory device.

1 174. (Amended) The method of claim 163 wherein the memory
2 device outputs the data onto an external bus.

1 175. (Amended) The method of claim 174 wherein the external
2 bus includes a set of signal lines to carry multiplexed address
3 information, data and control information.

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1 176. (Amended) A method of controlling a synchronous memory
2 device by a memory controller, wherein the memory device includes
3 an array of memory cells and a programmable register, the method of
4 controlling the memory device comprises:

5 providing a first operation code to the memory device, wherein
6 the first operation code initiates an access of the programmable
7 register in the memory device in order to store a binary value;

8 providing the binary value to the memory device, wherein the
9 memory device stores the binary value in the programmable register
10 in response to the first operation code;

11 providing a second operation code to the memory device,
12 wherein the second operation code instructs the memory device to
13 accept data that is issued by the memory controller;

14 providing a first portion of the data to the memory device in
15 response to a rising edge transition of the external clock signal;
16 and

17 providing a second portion of the data to the memory device in
18 response to a falling edge transition of the external clock signal.

1 177. (Amended) The method of claim 176 wherein the binary
2 value is representative of a delay time to transpire before the
3 memory device samples the data, and wherein the first portion of
4 the data is provided to the memory device after the delay time
5 transpires.

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~~178. (Amended) The method of claim 176 wherein the binary~~
2 value is representative of a number of clock cycles of the external
3 clock signal to transpire before the memory device samples the
4 data, and wherein the first portion of the data is provided to the
5 ~~memory device after the delay time transpires.~~

179. (Amended) The method of claim 176 wherein the binary
2 value is representative of a delay time to transpire before the
3 memory device outputs data in response to an operation code which
4 instructs the memory device to output data.

180. The method of claim 176 further including:
2 providing block size information to the memory device, wherein
3 the block size information defines an amount of data to be accepted
4 by the memory device in response to the second operation code.

181. The method of claim 176 further including providing
2 address information to the memory device.

182. The method of claim 181 wherein the address information
2 and the second operation code are included in a write request
3 packet.

183. (Amended) The method of claim 176 wherein the first
2 operation code and the data are provided to the memory device via
3 an external bus.

1 184. (Amended) The method of claim 183 wherein the external
2 bus includes a set of signal lines used to carry multiplexed
3 address information, the data and control information.

C1 1 185. The method of claim 176 wherein the second operation code
2 includes precharge information.

1 186. (Amended) A synchronous memory device, wherein the memory
2 device includes an array of memory cells, the memory device
3 comprises:

4 input receiver circuitry to sample a first operation code in
5 response to a first transition of an external clock signal;

6 a programmable register to store a binary value in response to
7 the first operation code, wherein the binary value is
8 representative of an amount of time to transpire before the memory
9 device outputs data; and

10 output driver circuitry to output data in response to a second
11 operation code and after the amount of time transpires, wherein a
12 first portion of the data is output in response to a second
13 transition of the external clock signal and a second portion of the
14 data is output in response to a third transition of the external
15 clock signal.

1 187. The memory device of claim 186 wherein the binary value
2 is representative of a number of clock cycles of the external clock
3 signal.

1 188. (Amended) The memory device of claim 186 wherein the
2 second transition of the external clock signal is a rising edge
3 transition and the third transition of the external clock signal is
4 a falling edge transition.

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1 189. (Amended) The memory device of claim 188 wherein the
2 second and third transitions of the external clock signal are
3 consecutive transitions.

1 190. The memory device of claim 189 wherein the first
2 operation code and the binary value are included in a packet.

1 191. The memory device of claim 190 wherein the first
2 operation code and the binary value are included in the same
3 packet.

1 192. (Amended) The memory device of claim 186 further
2 including delay lock loop circuitry to generate a first internal
3 clock signal, wherein the data is output in response to the first
4 internal clock signal.

1 193. (Amended) The memory device of claim 186 wherein the
2 input receiver circuitry receives address information.

1 194. (Amended) The memory device of claim 186 wherein the
2 output driver circuitry outputs the data onto an external bus
3 having a set of signal lines used to carry multiplexed address
4 information, the data and control information.

1 195. The memory device of claim 194 wherein the input receiver
2 circuitry samples the first operation code from the external bus.

1 196. The memory device of claim 186 wherein the output driver
2 circuitry and the input receiver circuitry are connected to a
3 common pad.

1 197. (Amended) The memory device of claim 186 wherein the
2 memory device is a synchronous dynamic random access memory.